IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method of operating a network device, comprising:

receiving electronic data from a first port of the data networking device;

deleting at least a portion of the electronic data prior to providing the electronic data to a memory of the networking device;

providing at least a portion of the electronic data to a second port;

generating a CRC (cyclic redundancy code), wherein the electronic data is to comprise a frame; [[and]]

inserting the CRC into the frame prior to providing to the memory; and

checking the CRC prior to providing to the second port.

2. (Currently Amended) The method of claim 1, further comprising modifying the electronic data prior to said providing to the second port.

3. (Canceled)

4. (Original) The method of claim 1, wherein the portion of electronic data deleted comprises a VLAN (virtual local area network) tag.

5. (Previously Presented) The method of claim 2, wherein modifying comprises inserting a VLAN tag to the frame.

6. (Canceled)

7. (Original) The method of claim 1, further comprising providing a portion of the electronic data to a control module prior to deleting a portion of the electronic data.

8. (Original) The method of claim 7, wherein the portion of data provided to the control module comprises the protocol header.

9. (Original) The method of claim 1, wherein the first port and the second port comprise a receive port and a transmit port, respectively.

10. (Currently Amended) An apparatus, comprising:
one or more receive ports capable of receiving electronic data from a network;
one or more transmit ports capable of transmitting electronic data to a network;
a memory; and
a processor, the processor configured to, in operation:
delete at least a portion of the electronic data received by the one or more receive ports;
provide the remaining electronic data to the memory;
read the electronic data from the memory;
modify the electronic data after reading from the memory; and
provide at least a portion of the electronic data to one or more of the transmit ports,
wherein the electronic data is to comprise a frame and wherein the processor is to cause generation of a CRC (cyclic redundancy code) and insertion of the CRC into the frame prior to storage in the memory, wherein the processor is to cause checking of the CRC prior to providing to the one or more transmit ports.

11. (Original) The apparatus of claim 10, wherein the processor is further configured to modify the electronic data prior to providing at least a portion of the electronic data to one or more of the transmit ports.

12. (Original) The apparatus of claim 10, wherein the apparatus comprises a network switch.

13. (Original) The apparatus of claim 12, wherein said memory comprises network switch internal memory.

14. (Original) The apparatus of claim 10, wherein said portion of electronic data deleted substantially comprises a VLAN tag.

15. (Original) The apparatus of claim 11, wherein modifying the electronic data comprises inserting a VLAN tag, wherein the VLAN tag relates at least in part to the destination address of the electronic data.

16. (Original) The apparatus of claim 10, wherein the processor comprises a network processor.

17. (Original) The apparatus of claim 10, wherein the memory comprises a plurality of memory devices.

18. (Original) The apparatus of claim 17, wherein the plurality of memory devices comprise one or more of: random access memory, static random access memory, and synchronous dynamic random access memory.

19. (Currently Amended) A system for network data communication, comprising:

a first port to receive electronic data from a network;

a second port to transmit electronic data to a network;

a memory to store electronic data; and

a processor coupled to the first port, second port, and the memory, wherein the processor is configured to, in operation, delete at least a portion of electronic data received on a first port, provide at least a portion of the electronic data to the memory, and modify the electronic data prior to providing at least a portion of the electronic data to the second port, wherein the electronic data is to comprise a frame and wherein the processor is to cause generation of a CRC (cyclic redundancy code) and insertion of the CRC into the frame prior to storage in the memory, wherein the processor is to cause checking of the CRC prior to providing to the second port.

20. (Canceled)

21. (Original) The system of claim 19, wherein the portion of electronic data deleted comprises a VLAN (virtual local area network) tag.

22. (Canceled)

23. (Original) The system of claim 19, wherein modifying the electronic data comprises inserting a VLAN tag, wherein the VLAN tag relates at least in part to the destination address of the electronic data.

24. (Original) The system of claim 19, wherein the processor comprises a network processor.

25. (Original) The system of claim 19, wherein the memory comprises a plurality of memory devices.

26. (Original) The system of claim 25, wherein the plurality of memory devices comprise one or more of: random access memory, static random access memory, and synchronous dynamic random access memory.

27. (Original) The system of claim 19, wherein said processor is configured to modify said electronic data only if said second port is configured to recognize tags.

28. (Currently Amended) The method of claim [[10]] 1, further comprising, in response to deleting the portion of the electronic data, generating a CRC (cyclic redundancy code) of an undeleted portion of the electronic data.

29. (Previously Presented) The apparatus of claim 10, wherein the processor is to generate a CRC (cyclic redundancy code) of an undeleted portion of the electronic data.

30. (Previously Presented) The system of claim 19, wherein the processor is to generate a CRC (cyclic redundancy code) of an undeleted portion of the electronic data.

31. (New) The method of claim 1, wherein the memory is internal to the network device.

32. (New) The apparatus of claim 10, wherein the memory comprises an internal memory.

33. (New) The system of claim 19, wherein the memory comprises an internal memory.